Cell Library Introduction

[image of cell globals here]

The set of cells contained within this library are based upon 0.35µm unified CMOS technology. The follow a two-layer metal design ontop of a p-type substrate with N-Well and P-Well regions for pull-up and pull-down networks respectively. All cells are a common 17.2µm high, with varied widths all integer multiples of 1.2µm.

All transistors are fixed at : WP = 2.4µm LP = 0.35µm

WN = 1.5µm LN = 0.35µm

Global signals and power rails are arranged horizontally in metal 1. While cell I/O signals are arranged vertically in metal2 and aligned to a 1.2µm grid.Power rails are 1.25um wide, while other horizontal signals are 0.5µm wide. The distance between hotizontal signals is 0.8µm from center to center. Both rails are formed using a continuous ohmic region and line of taps.

Vertical signals lines are 0.6um wide with position of each signal measured from the left edge of the cell to the right edge of the metal strip and detailed on each cell page.

AC characteristics of cells are measured as the propagation delay from each input to each output under normal operation conditions. This is set as having each input driven through one inverter and each output loaded by two inverters from this library. Each cell lists both the delay to correct output as a result of an input going high, as well as an input going low.

Major cells in the library have additional sections detailing the stick diagram and transistor layout of each cell as designed by the designated team member. Although only 4 members were in the group, both the half adder and XOR2 have been included in the library and detailed.